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REMARKS

Claim 1 to 19 are pending in this application; of which, claim 1 is the independent claim. Favorable reconsideration and further examination are respectfully requested.

Applicants acknowledge the Examiner's indication that claims 12 to 18 would be allowable if rewritten in independent form to include the base claim and any intervening claims; however, Applicants believe they are entitled to broader claims.

Claims 1 to 6, 10, 11 and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshida et al. (U.S. Patent 5,767,009).

Claim 1, as amended, is directed to a multi-layer integrated semiconductor structure. The multi-layer integrated semiconductor structure includes a first semiconductor structure including a first surface and semiconductor elements associated with a first semiconductor signaling technology. The multi-layer integrated semiconductor structure also includes a second semiconductor structure including a second surface and semiconductor elements associated with a second semiconductor signaling technology. The multi-layer integrated semiconductor structure further includes an interface disposed between the first surface and the second surface. The interface includes a first portion adapted to provide a communication interface between the first and second semiconductor structures and a second portion adapted to reduce electrical interference between signals propagating along the first and second semiconductor structures. The second portion is directly coupled to the first surface and the second surface. At least one of the first and second interface portions corresponds to a conductive bonding interface which

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secures the first surface of the first semiconductor structure to the first surface of the second semiconductor structure.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Yoshida does not disclose or suggest a second portion adapted to reduce electrical interference between signals propagating along the first and second semiconductor structures and directly coupled to the first surface and the second surface.

Specifically, Yoshida discloses an electro-conductive layer 18 disposed in between two semiconductor structures; however, the electro-conductive layer is not directly coupled to the two semiconductor structures, but rather sandwiched amongst other layers between the two semiconductor structures (see FIGS. 7B to 7D of Yoshida). Therefore, Yoshida does not disclose or suggest a second portion adapted to reduce electrical interference between signals propagating along the first and second semiconductor structures and directly coupled to the first surface and the second surface. For at least this reason, claim 1 is believed to be allowable.

Applicants submit that all dependent claims now depend on an allowable independent claim. For at least the foregoing reasons, Applicants request withdrawal of the art rejection.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper,

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and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the address below. Applicants' attorney can be reached by telephone at (781) 401-9988 ext. 23.

Enclosed in a Petition for a One-Month Extension of Time. No other fee is believed to be due for this Response; however, if any other fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: MIT-136DUS.

Respectfully submitted,

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Date: 3 NO1 2005

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